accumulating counts of the detected binary pulse voltage levels at the time ~~offsetss~~ offsets in a column and row point of the array[,] ; and

displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.

* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this Response C in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request reconsideration of the above referenced patent application in view of the remarks as set forth below.

Rejections under 35 U.S.C. §102

The Examiner has rejected claims 1 through 16 under 35 U.S.C. §102(a) as being anticipated by European Patent Application EP 1 143 654 A2 filed on March 4, 2001 by Thomas Eugene Waschura and James Roger Waschura and Robert Lee Verity (Waschura et al.). Applicant respectfully traverses the Examiner's rejection of applicant's claims 1 through 16 by Waschura et al. The Examiner has recited a number of rejections for applicant's claims 1 through 16. Applicant will consider each rejection independently.

It is to be noted that both the current application and Waschura et al. are assigned to SyntheSys Research, Inc., Menlo Park, California 94025 United States.

In rejecting claim 1 the Examiner states that Waschura et al. disclose " ... apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator ... and logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics ....". The Examiner's attention is drawn to paragraph [0012], lines 49 through 55 of the disclosure by Waschura et al. wherein it is clearly stated that "In a preferred embodiment ... apparatus for determining characteristics of a bit stream of binary pulses has measuring apparatus for sampling

pulse voltage levels in excess of voltage threshold levels ...". Waschura et al. further states, paragraph [0013], lines 7 through 13, that in accordance with his invention a "method ... generates a series of threshold voltage levels and ... accumulates ... counts of pulse voltage levels in excess of the generated voltage threshold levels ....". Applicant discloses apparatus and method in the disclosure and drawing having control means for defining a window comparator and logic means for accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator. Applicant's apparatus and method accumulates voltage counts of the bit stream pulses falling within voltage thresholds inside a window comparator. In contrast, Waschura et al. very clearly states that they accumulate counts of pulse voltage levels in excess of the generated voltage threshold levels. Applicant has amended claim 1 to recite "... logic means for accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator ....".

It is submitted that amended independent claim 1 is neither taught nor anticipated by the Waschura et al. reference and amended claim 1 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al. It is further submitted that dependent claims 2 through 6 further define the novel structure recited in amended parent claim 1 and that the apparatus recited therein is neither taught nor anticipated by the Waschura et al. reference and claims 1 through 6 are therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

In rejecting independent claim 7 the Examiner states that Waschura et al. disclose " ... apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator ... and apparatus for creating a voltage threshold window ... for accumulating counts of voltage levels of the binary pulses ... when the pulse voltage levels are within the voltage threshold window ....". As set forth above Waschura et al. discloses apparatus and method for sampling pulse voltage levels in excess of, not between, voltage threshold levels. The reference

by Waschura et al. discloses that that their apparatus and method generates a series of threshold voltage levels and accumulates counts of pulse voltage levels in excess of the generated voltage threshold levels. In contrast to Waschura et al., applicant's independent claim 7 recites " ... apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels ... for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.". It is submitted that Waschura et al. neither disclose, teach nor anticipate applicant's apparatus recited in claim 7 for accumulating counts of voltage levels of the binary pulses occurring within the voltage threshold window. It is to be noted that Waschura et al. is silent in this regard.

It is submitted that independent claim 7 is neither taught nor anticipated by the Waschura et al. reference and claim 7 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

In rejecting independent claim 8 the Examiner states that Waschura et al. disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising first and second control, logic, first and second counter means and monitor apparatus. Applicant's independent claim 8 recites "... first control means for defining a window comparator ...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold ... logic means for detecting voltage levels of the binary pulses ... when the pulse voltage levels are within the voltage threshold ... and monitor apparatus for displaying ... accumulated time and voltage counts as an eye diagram ....". It is submitted that Waschura et al does not disclose, teach nor anticipate this recited structure for detecting voltage levels of the binary pulses when the pulse voltage levels are within the voltage thresholds. In contrast, Waschura et al., as set forth in their disclosure and drawing, Fig. 2, above threshold counter 203, sample voltage levels in excess of voltage threshold levels.

Thus, it is submitted that independent claim 8 is neither taught nor anticipated by the Waschura et al. and claim 8 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

In rejecting independent claim 9 the Examiner states that Waschura et al. discloses the steps of defining a window comparator and accumulating event counts. As set forth in the disclosure and in the drawing, applicant's method accumulates various voltage counts of voltage levels of the bit stream pulses within voltage thresholds and draws an eye diagram therefrom defining the bit stream pulse characteristics. In contrast, the reference by Waschura et el., as set forth above, teaches a method that samples voltage levels in excess of voltage threshold levels, paragraph [0011], lines 37 through 41, and drawing Fig. 2, above threshold counter 203 of control 21. Applicant has amended independent claim 9 to recite the step of "accumulating various voltage counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics".

It is submitted that amended independent claim 9 is neither taught nor anticipated by Waschura et al. and amended independent claim 9 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al. It is further submitted that dependent claims 10 through 14 further define the novel method recited in amended parent claim 9 and that the method steps recited therein are neither taught nor anticipated by Waschura et al. and claims 9 through 14 are therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

In rejecting independent claim 15 the Examiner states that Waschura et al. discloses the steps of defining a window comparator, creating a voltage threshold window, accumulating counts of binary pulse voltage levels and displaying the accumulated voltage counts as an eye diagram. In contrast to Waschura et al., applicant's independent claim 15 recites a novel method comprising steps of defining a window comparator of an array defining points for accumulating event counts of the

binary pulse bit stream, creating a voltage threshold window that moves between a minimum voltage and a maximum voltage at each row of the array, and accumulating counts of voltage levels of the binary pulses when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the accumulated event counts as an eye diagram. As set forth above and in accordance with their disclosure and drawing, Waschura et al. teaches a method that samples voltage levels in excess of voltage threshold levels, paragraph [0011], lines 37 through 41, and drawing Fig. 2, above threshold counter 203 of control 21. Applicant's novel method recited by claim 15 recites the steps of "... creating a voltage threshold window that moves between a minimum voltage and a maximum voltage ...and accumulating counts of voltage levels of the binary pulses ... when the pulse voltage levels are within the voltage threshold window ... and displaying the ... accumulated ... counts as an eye diagram ....". It is submitted that Waschura et al. do not disclose, teach nor anticipate these novel steps of applicant's novel method recited by claim 15 and are totally silent in regards thereto.

It is submitted that independent claim 15 is neither taught nor anticipated by Waschura et al. and claim 15 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

In rejecting independent claim 16, the Examiner states that Waschura et al. discloses the steps of defining a window comparator, creating a voltage threshold window, detecting voltage levels of the binary pulses, accumulating counts of the detected binary pulse voltage levels and displaying an eye diagram defining characteristics of the bit stream of binary pulses. Applicant's independent claim 16 recites the novel method steps of " ... defining a window comparator of an array ... defining points for accumulating event counts ...during defined duration times of the binary pulse bit stream ... creating a voltage threshold window that moves between defined voltage levels at each row of the array ...detecting voltage levels of the binary pulses occurring ... when the pulse voltage levels are within the voltage threshold window at each row and column point of the array ... accumulating counts of the

detected binary pulse voltage levels at ... time offsets in... the array, and displaying ... accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.". In contrast to applicant's method recited in claim 16, Waschura et al., as set forth in their disclosure and drawing, do not, as recited by applicant's claim 16, create a voltage threshold window that moves between defined voltage levels at each row of the array and detect voltage levels of the binary pulses occurring when the pulse voltage levels are within the voltage threshold window, i.e., between defined voltage levels, at each row and column point of the array, accumulating counts of the detected binary pulse voltage levels and displaying the counts as an eye diagram. Waschura et al. differs by accumulating multiple counts of the sampled pulse voltage levels in excess of, not within, threshold voltage levels. Waschura et al do not disclose, teach or anticipate applicant's claimed method recited in claim 16 as having the steps of creating a voltage threshold window that moves between defined voltage levels, detecting and accumulating voltage levels of the binary pulses occurring when the pulse voltage levels are within the voltage threshold window between the defined voltage levels and displaying the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses. Waschura et al. is noted for its silence in this regard.

It is submitted that independent claim 16 is neither taught nor anticipated by Waschura et al. and claim 16 is therefore clearly allowable under 35 U.S.C. 102(a) in view of the reference by Waschura et al.

Regarding dependent claims 2 through 6 and 10 through 14, it is submitted that dependent claims 2 through 6, further defining the apparatus recited in amended parent claim 1, and dependent claims 10 through 14, further defining the method recited in amended parent claim 9, are neither taught nor anticipated by Waschura et al. and are clearly allowable under 35 U.S.C. 102(a).

In summary, both applicants' claimed invention and the reference by Waschura et al. relate to different apparatus and methods for measuring the characteristics of a serial bit stream of binary pulses. Neither, although having a common inventor,

anticipates the other and both compliment each to improve the art in measuring the ability of transmission facilities to transmit and receive high speed serial binary bit streams.

In view of the above set forth arguments it is submitted that claims 1 through 16 are neither taught nor anticipated by the Waschura et al. reference and are therefore clearly allowable under 35 U.S.C. 102(a).

CONCLUSION

In summary, the Examiner has again rejected claims 1 through 16. In view of the arguments herein set forth and the amendment of independent claims 1 and 9, applicant respectfully submits that claims 1 through 16 distinguish over the art cited by the Examiner and are allowable. Applicant having answered each and every ground of rejection as set forth by the Examiner submits that the case is in condition for allowance and the same is respectfully solicited. Favorable action in that regard and passage of this case to issue are earnestly solicited.

If any questions should arise with respect to the above remarks, or if it would in any way expedite the prosecution of this case, applicants' attorney would appreciate a telephone call by dialing Area Code (408)-965-4001.

Respectfully submitted

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